

REMARKS

In the Final Office Action of August 4, 2008, claims 1-5 and 7-12 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over U.S. Patent No. 4,527,255 (“Keshtbod”) in view of U.S. Patent No. 6,363,011 (“Hirose et al.”).

In response, Applicant respectfully asserts that the independent claim 1 is not obvious in view of the cited references of Keshtbod and Hirose et al., as explained below. In view of the following remarks, Applicant respectfully requests that the pending claims 1-5 and 7-12 be allowed.

I. Patentability of Independent Claim 1

The independent claim 1 was rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Keshtbod in view of Hirose et al. However, Examiner has failed to establish a *prima facie* case of obviousness for the independent claim 1. Thus, Applicant respectfully asserts that the independent claim 1 is not obvious in view of the cited references of Keshtbod and Hirose et al. As such, Applicant respectfully requests that the independent claim 1 be allowed.

The Office Action admits on page 4 that the cited reference of Keshtbod does not disclose that “the static memory means comprises a pair of cross-coupled inverters.” The Office Action then states that “Hirose et al. teaches the static memory (**Fig. 4, #4**) means comprises a pair of cross-coupled inverters (**Fig. 1, #45, #45’**).” The Office Action then alleges that “[i]t would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Hirose et al. to the teaching of Keshtbod such that the reading process of six transistors SRAM cells is easier than four transistors SRAM cells.”

First, Applicant does not fully understand the statement “such that the reading process of six transistors SRAM cells is easier than four transistor SRAM cells,” which appears to be the alleged motivation to apply the inverters 45 and 45’ of Hirose et al. to the bi-stable memory cell 30 of Keshtbod. This statement seems to suggest that the reading process of six transistors SRAM cells (presumably, the resulting

memory cell) is somehow easier than the reading process of four transistors SRAM cells. Applicant fails to see how the reading process involving more transistors can be easier than the reading process involving fewer transistors. “The key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious.” MPEP §2142. In the case at hand, the Office Action has not provided a clear articulation of the reason(s) why it is obvious to apply the teachings of Hirose et al. to the teachings of Keshtbod. Thus, the Office Action has not provided sufficient support to render the independent claim 1 obvious.

Second, there is no reasonable expectation of success in applying the teachings of Hirose et al. to the teachings of Keshtbod by presumably modifying the bi-stable memory cell 30 of Keshtbod using the inverters 45 and 45' of Hirose et al. The prior art can be modified or combined to reject claims as *prima facie* obvious as long as there is a reasonable expectation of success. *In re Merck & Co., Inc.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Applicant notes herein that parts of a circuit cannot just be added to another circuit without knowing how those parts will function in the latter circuit. In certain situations, it cannot be known unless simulations are performed. In the case at hand, there is no reasonable expectation that adding the inverters 45 and 45' of Hirose et al. into the bi-stable memory cell 30 of Keshtbod would be successful since the inverters 45 and 45' of Hirose et al. are used with transistors 43 and 43', which are configured differently than transistors Q3 and Q4 of the bi-stable memory cell 30 of Keshtbod. Thus, there is no reasonable expectation that the inverters 45 and 45' of Hirose et al. will function properly with the transistors Q3 and Q4 of the bi-stable memory cell 30 of Keshtbod.

Third, even assuming that there is reasonable expectation of success, the principle of operation of the memory cell of Keshtbod will be changed with the proposed modification. If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959). The inclusion of the inverters 45 and 45' of Hirose et al. to the bi-stable memory cell 30 of Keshtbod would presumably require a Src signal, which is applied to the inverters 45 and 46', as illustrated in Fig. 4 of Hirose et al. Since the bi-stable memory cell 30 of Keshtbod

does not use such a signal for operation, the principle of operation of the memory cell of Keshtbod would need to be changed if the inverters 45 and 45' of Hirose et al. are included in the bi-stable memory cell 30 of Keshtbod. Thus, since the proposed modification of the bi-stable memory cell 30 of Keshtbod would change the principle of operation of the bi-stable memory cell, the teachings of Keshtbod and Hirose et al. are not sufficient to render the independent claim 1 *prima facie* obvious.

For all the above reasons, Applicant respectfully asserts that the independent claim 1 cannot be rendered obvious in view of the cited references of Keshtbod and Hirose et al. As such, Applicant respectfully requests that the independent claim 1 be allowed.

II. Patentability of Dependent Claims 2-5 and 7-12

Each of the dependent claims 2-5 and 7-12 depends on the independent claim 1. As such, these dependent claims include all the limitations of the independent claim 1. Therefore, Applicant submits that these dependent claims are allowable for at least the same reasons as the independent claim 1.

Applicant respectfully requests reconsideration of the claims in view of the remarks made herein. A notice of allowance is earnestly solicited.

Respectfully submitted,
Roger Cuppens

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By: /thomas h. ham/
Thomas H. Ham
Registration No. 43,654
Telephone: (925) 249-1300